THE CASCADE: Implementation Results

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- Proof-Of-Concepts (PoCs)
- 2 Hardware Implementations
- Fault Attacks

Conclusion and Future Works



PoCs Platforms

2 Arduinos Mega2560 (256kB Flash, 8kB SRAM, 4kB EEPROM)

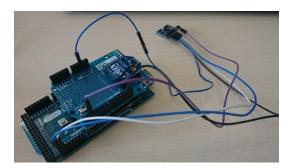
Fault Attacks

- ► Each one integrates 1 XBee module for radio communications
- ▶ (optional: sensing environmental data temperature, acceleration, etc.)
- ▶ PoCs implementing LPV-SSSC with dimension = 7
 - Also available in dimension 40



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Outline

COM32 (Arduino/Genuino Mega or Mega 2560) Envoyer SHI~ SLW Set configuration Command successful IDe15 Command successful DM 3 Command successful - EE 1 Command successful Command successful Command successful SETUP FINISHED! Sending data... Raw Dates to Encrypt: Simple Demo! True Datas to Encrypt (HEX values with padding): 8310D053696D706C652044656D6F210093 Data encrypted: 9900040F41D559C7A1D64983B4C64BA638 Q~ ECn Data sent

Pas de fin de ligne → 9600 baud →





☑ Déflement automatique

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Erroneous Communications





Traffic Analysis (1/2)

```
Chrover
 Command successful
SETUP PERISSEDS
Nav Datas to Encrypt: Traffic Analysis! Results incoming.
True Dates to Entruto (SEE values with reddings): $310004726160060053204165616C79756973212052679756C7473206965698698867250093
 Data encrypted: 990CC4CF443C39938146CB4C9AD77CTB03711E253D75175EF24B7DE365CEAC137C2C0EB66FDAB95B
Naw Dates to Encrypt: Traffic Analysis: Results incoming.
 True Datus to Encrypt (HEE values with pedding): D31000472016666696320416E616C797369732120526573756C747320898E636F6898E672E0093
Data encrused: B4351FlaciB4ac34E55c431D0CDxD035351E314E087276BEE478631ATD002F00D000270CAC0EA
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```

```
- 0 -
                                                                                        Envoyer
    SET- SIN
Set configuration
 CE_
Command successful
 - IDeff
Command successful
  DE 5
Command successful
 EE 1
Command successful
Command successful
- 9836
Command successful
SETUP FINISHED!
Data received: 990004CF461C39938146CB4C9AD7TC7803711E253D75175EF24B7DE3855EAC137C2C3EB88FTAB95B
Data decrypted: 995CD5D05472616466694320416E616C797369732120526573756C747320694E636F6D694E672E00
Raw Data decrypted: Traffic Analysis! Results incoming.
Data received: B6250F5AC084AC36E55C430D3CD4D825351E314E83A7276AEE47A631A7FD902F60CB0C027BCAC0EA
Data decrypted: 938310005472616666696320416E616C797369732120526573756C747320696E636F6D696E672E00
Raw Data decrypted: Traffic Analysis! Results incoming

☑ Défiement automatique

                                                                    Pas de fin de ligne - 9500 baud -
```



Traffic Analysis (2/2)

Data encrypted: 8DAE314A5E7A355A590E8B6D5ABB9BD5B6CCDB6344362D22AE099AD7BEB1C96E0FBE598112C25CC3 Data encrypted: 2171DBF569A247C8670DC7865042A95355535D4CCB43C15FD66BBF796E465D3F0C29A57D86793D37



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 - ► AES-CFB (Cipher Feedback): 128×10 = 1280 cc
 - ► MOUSTIQUE: 96 cc
 - ► LPV-SSSC: 40 cc



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- ▶ It is a kind of "magic" when it is synchronizing...



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SAKURA-G

- ► (Japanese) platform dedicated to side-channel evaluation
- ► Spartan-6 LX75: 11662 Slices (4 6-input LUTs + 8 1-bit register), BRAM: 172 × 18 Kb, DSP Blocks: 132

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Implemented Versions

- "Enc. Full/Dec. Full": Full encryption/decryption version in dimension 40 with 781 SBoxes
- ► "Enc.+Dec. Full": Combination of previous encryption and decryption components
- ► "Enc./Dec. r1": Reduced version with one specific 80 SBoxes instantiation
- ► "Enc./Dec. r2": Reduced version with another specific 80 SBoxes instantiation
- "Folded Version": only 1 line implemented
- ► GRAIN128, Trivium: eSTREAM candidates (synchronous stream ciphers)



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Implementation Results

Outline

LUTs Version Slices Freq. (MHz) TP (Mbps) Enc. Full Dec. Full Enc.+Dec. Full Enc. r1 Dec. r1 Enc. r2 Dec. r2 Folded Version **GRAIN128**

Implementation Details

Trivium

Spartan-6 LX75, Post-P&R, Area Optim., TP (Throughput)

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Hardware Implementations

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Main Lessons

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 - Variant exists that would increase this reuse rate, but decrease encryption performance
- ► Relatively slow compared to competitors due to longer datapath
 - ▶ Due to XOR sum of the line components of the internal state



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 - Simultaneous 4-bit stuck-at 0 value faults



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- From random to precise bit errors
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 - Simultaneous 4-bit stuck-at 0 value faults
- ► Single fault (1st order) vs. Multiple faults (2nd order+)

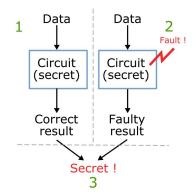
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DFA

Definition (DFA)

DFA = Differential Fault Analysis

pairs of faulty/correct ciphertexts are needed





LPV SSSC Properties

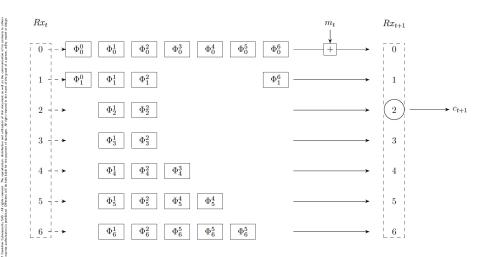
Notations

- Register Rx containing n nibbles x[i] initialized with an internal IV
- Key length $\frac{4\times(n+s+r)}{2}$ bits, with:
 - s: number of encrypted symbols used in the update function
 - r: relative degree
- $\triangleright x'[i]$: faulted value of x[i] and $\Delta x[i]$ the difference x[i] + x'[i]
- δ_i : initial difference (i.e. $x_t'[i] = x_t[i] + \delta_i$)
- c': faulted encrypted symbol

Parameters

- ightharpoonup n = 7, r = 3, s = 1, bijective S-Box S
- Master Key length: 22 bits, derivated into 22 4-bit subkeys SKi
 - ▶ Toy example with further extensions for n = 40 in mind

Encryption Routine



One Round Encryption by LPV-SSSC

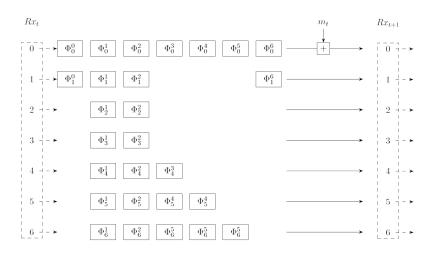
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DFA Principle

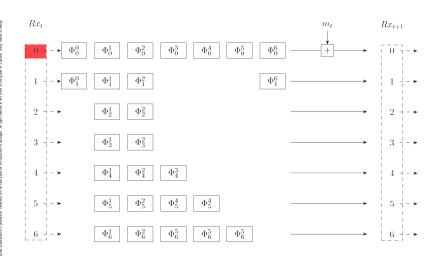
- Study the differences on the encrypted symbols between a normal and faulted execution, with a fault injected on x[i]
 - System of equations obtained
 - Extraction of subkey bits by solving the system
- ► More precisely, obtain linear equations with the *SK*_is
 - ▶ Eliminate some unknown values with the available linear equations
 - Obtain additional linear equations by injecting the variables computed before in quadratic equations



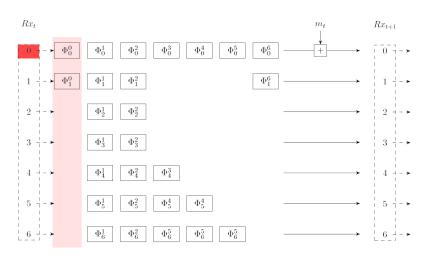
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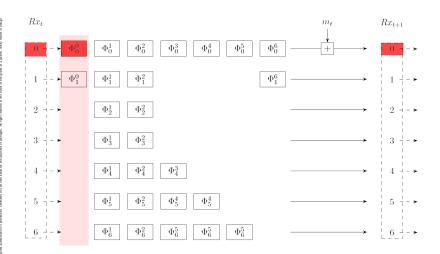
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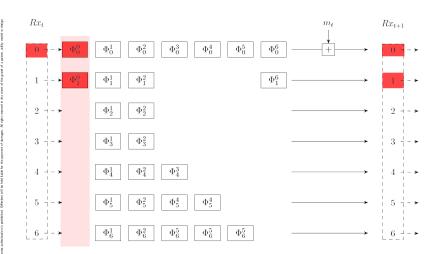


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Fault Diffusion Example



Fault Diffusion on $x_t[0]$

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Example: Fault Injected on
$$x_t[0]$$
 (i.e. $\Delta x_t[0] = \delta_0$)

$$x_{t+1}[0] = \sum_{j=0}^{6} S(c_t + SK_j) \cdot x_t[j]$$



Hardware Implementations

$$x_{t+1}[0] = \sum_{j=0}^{6} S(c_t + SK_j) \cdot x_t[j]$$

$$\implies \Delta x_{t+1}[0] = \Delta (\sum_{j=0}^{6} S(c_t + SK_j) \cdot x_t[j])$$



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$$= \sum_{j=0}^{6} S(c_t + SK_j) \cdot \Delta x_t[j]$$

$$= \delta_0 \cdot S(c_t + SK_0) + \sum_{j=1}^{6} S(c_t + SK_j) \cdot 0$$



$$x_{t+1}[0] = \sum_{j=0}^{6} S(c_t + SK_j) \cdot x_t[j]$$

$$\Rightarrow \Delta x_{t+1}[0] = \Delta \left(\sum_{j=0}^{6} S(c_t + SK_j) \cdot x_t[j]\right)$$

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$$= \delta_0 \cdot S(c_t + SK_0)$$

Example: Fault Injected on $x_t[0]$ (i.e. $x_t'[0] = x_t[0] + \delta_0$)

Cycle *t*:

$$\Delta x_{t+1}[0] = \delta_0 \cdot S(c_t + SK_0)$$

$$\Delta x_{t+1}[1] = \delta_0$$

$$\Delta x_{t+1}[2] = 0$$

$$\Delta x_{t+1}[3] = 0$$

$$\Delta x_{t+1}[4] = 0$$

$$\Delta x_{t+1}[5] = 0$$

$$\Delta x_{t+1}[6] = 0$$



Fault on $x_t[0]$ (i.e $x_t'[0] = x_t[0] + \delta_0$)

 $\Delta x_{t+2}[6] = \delta_0 \cdot S(c_{t+1} + SK_{17})$

Cycle t+1:

$$\Delta x_{t+2}[0] = \delta_0 \cdot [S(c_{t+1} + SK_0) \cdot S(c_t + SK_0) + S(c_{t+1} + SK_1)]$$

$$\Delta x_{t+2}[1] = \delta_0 \cdot [S(c_t + SK_0) + 1]$$

$$\Delta x_{t+2}[2] = \delta_0$$

$$\Delta x_{t+2}[3] = \delta_0 \cdot S(c_{t+1} + SK_8)$$

$$\Delta x_{t+2}[4] = \delta_0 \cdot S(c_{t+1} + SK_{10})$$

$$\Delta x_{t+2}[5] = \delta_0 \cdot S(c_{t+1} + SK_{13})$$

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Fault Attacks

Remarks

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- 2. Subkeys are involved always at the same positions, however the attacker can only access to the 3^{rd} line
 - → Observability problem
- 3. Once the produced encrypted symbol is faulted, we get x[i] terms in equations Δ after two iterations
 - → Limited number of exploitable equations for one fault



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SK₀, SK₆, SK₇ Recovery

▶ Random fault on $x_t[0]$:

$$\left\{ egin{aligned} \Delta c_{t+2} &= \delta_0 \ \Delta c_{t+3} &= \delta_0 \cdot \mathrm{S}(c_t + \mathrm{SK}_0) \end{aligned}
ight.$$



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ightharpoonup Random fault on $x_t[0]$:

$$\begin{cases} \Delta c_{t+2} = \delta_0 \\ \Delta c_{t+3} = \delta_0 \cdot \mathrm{S}(c_t + \mathrm{SK}_0) \end{cases}$$

Hardware Implementations

$$\rightarrow \mathrm{SK}_0 = \mathrm{S}^{-1} \big(\Delta c_{t+3} \cdot (\Delta c_{t+2})^{-1} \big) + c_t$$



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$$\rightarrow SK_0 = S^{-1}(\Delta c_{t+3} \cdot (\Delta c_{t+2})^{-1}) + c_t$$

► Same principle for SK₆ and SK₇



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(SK_1, SK_{17}) and (SK_2, SK_{18}) Recovery

▶ For a random fault on $x_t[0]$, at cycle t + 4:



(SK_1, SK_{17}) and (SK_2, SK_{18}) Recovery

▶ For a random fault on $x_t[0]$, at cycle t + 4:

$$\mathrm{S}(c_{t+1}+\mathrm{SK}_1)+\mathrm{S}(c_{t+1}+\mathrm{SK}_{17})=f_0(\delta_0,\mathrm{SK}_0,\mathrm{SK}_7,c_i,c_i')$$



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▶ For a random fault on $x_t[0]$, at cycle t + 4:

$$S(c_{t+1} + SK_1) + S(c_{t+1} + SK_{17}) = f_0(\delta_0, SK_0, SK_7, c_i, c_i')$$

- \rightarrow 16 possible candidates for (SK₁, SK₁₇), because of the Sbox bijectivity
- ▶ Random fault on $x_t[1]$ or on $x_t[6]$: new set of 16 possible couples for $(SK_1, SK_{17}).$



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 - \rightarrow By intersecting the sets, two candidates for the couple $(SK_1, SK_{17}).$
- Same principle to recover (SK₂, SK₁₈)



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(SK5, SK21), (SK4, SK16, SK20), (SK3, SK12, SK15, SK19) Recovery

▶ Random fault on $x_t[5]$:

$$\begin{cases} \Delta c_{t+3} = \delta_5 \cdot [S(c_t + SK_5) + S(c_t + SK_{21})] \\ \Delta c_{t+4} = \delta_5 \cdot [S(c_{t+1} + SK_0) \cdot S(c_t + SK_5) + S(c_{t+1} + SK_6) \cdot S(c_t + SK_{21})] \end{cases}$$



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(SK5, SK21), (SK4, SK16, SK20), (SK3, SK12, SK15, SK19) Recovery

▶ Random fault on $x_t[5]$:

$$\begin{cases} \Delta c_{t+3} = \frac{\delta_5}{5} \cdot [S(c_t + SK_5) + S(c_t + SK_{21})] \\ \Delta c_{t+4} = \frac{\delta_5}{5} \cdot [S(c_{t+1} + SK_0) \cdot S(c_t + SK_5) + S(c_{t+1} + SK_6) \cdot S(c_t + SK_{21})] \end{cases}$$

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 - ▶ For each δ_5 , 1 solution for (SK_5, SK_{21})
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- \rightarrow 15 possibilities for δ_5
 - ▶ For each δ_5 , 1 solution for (SK_5, SK_{21})
 - $ightharpoonup \to 15$ possible candidates for $(\delta_5, SK_5, SK_{21})$
- ► Same principle for (SK4, SK16, SK20) and (SK3, SK12, SK15, SK19) recovery, except that we got more hypothesis to test since we face more unknown values

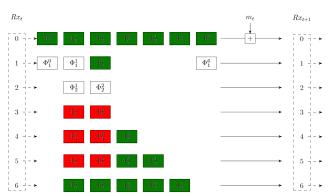


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Subkeys Required Faults SK_0 1 on x[0] SK_7 1 on x[2] SK_6 1 on x[6] (SK_1, SK_{17}) 1 on x[1](SK₂, SK₁₈) 2 on x[2](SK₅, SK₂₁) 3 on x[5](SK₄, SK₂₀) 3 on x[4] $(SK_3, SK_{12}, SK_{15}, SK_{19})$ 5 on x[3]Total 17



Summary of the Obtained Subkeys



- ► Remaining red subkeys can be obtained thanks to a stronger attack model (Simultaneous 4-bit stuck-at 0 value faults + more precise location)
- Around 20 faults to recover all the subkeys

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- ► (Fast) synchronization is a very nice property in crypto but it can come with a high cost
 - 2.5 bigger than Trivium
- ► Limited overhead to combine both encryption and decryption
 - ▶ Variants are also possible to have a near 100% reuse
- Intrinsic protection against side-channel attacks when initial state is unknown by the attacker
 - (see Brandon Dravie's presentation)
- ▶ DFAs in dimension 7 are possible, seems very much more difficult in dimension 40
 - (due to very fast fault diffusion)



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Future Works

Hardware

- ► Side-channel protection with Threshold Implementation (costly) and (1st-2nd order) analysis on FPGA/SAKURA-G
- ► ASIC (CMOS 90nm) implementations for a deeper comparison

Software

- Side-channel protection and (1st-2nd order) analysis on ATMega smart cards
- ► Give throughput benchmarks on different platforms

Fault Attacks

► Extend the analysis done in dimension 7 to dimension 40 (not easy!)

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